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| Program: Bachelor of Science Honours (Information Technology) | Semester: II |
| Course: Electronics & Communication Technology II | Code:  |
| Teaching Scheme | Evaluation Scheme |
| Lecture | Practical | Tutorial | Credits | Theory | Practical |
| Internal | External | Internal | External |
| 45 | Nil | Nil | 03 | 40 | 60 | Nil | Nil |
|   |
| Internal Component  |
| Class Test Duration Mins | Assignment& projects |  Class Participation |
|  20 Marks  | 20 | Nil |
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| Learning Objectives1. To equip students with the fundamental knowledge and basic technical competence in the field of Microprocessors.
2. To emphasize on instruction set and logic to build assembly language programs.
3. To prepare students for higher processor architectures and embedded systems
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| Learning Outcomes1. Describe core concepts of 8086 microprocessor.
2. Interpret the instructions of 8086 and write assembly and Mixed language programs.
3. Identify the specifications of peripheral chip and design 8086 based system using memory and peripheral chips.
4. Appraise the architecture of advanced processors
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| Pedagogy* PPTs, Case studies, Group discussions, Classroom Activity, Videos, Research papers, News articles etc.
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**Module I (11)**

**The Intel Microprocessors 8086 Architecture**

8086CPU Architecture, Programmer’s Model, Functional Pin Diagram, Memory Segmentation, Banking in 8086, Demultiplexing of Address/Data bus, Functioning of 8086 in Minimum mode and Maximum mode, Timing diagrams for Read and Write operations in minimum and maximum mode, Interrupt structure and its servicing

**Module 2**   **(12)**

 **Instruction Set and Programming**

Addressing Modes, Instruction set-Data Transfer Instructions, String Instructions, Logical Instructions, Arithmetic Instructions, Transfer of Control Instructions, Processor Control Instructions,Assembler Directives and Assembly Language Programming, Macros, Procedures

**Module 3 (12) Memory and Peripherals interfacing**

Memory Interfacing - RAM and ROM Decoding Techniques – Partialand Absolute, 8255-PPI-Block diagram, CWR, operating modes, interfacing with 8086. 8257-DMAC-Block diagram, DMA operations and transfer modes.Programmable Interrupt Controller 8259-Block Diagram, Interfacing the 8259 in single and cascaded mode.

**Module 4 (10)**

**Pentium Processor 6**

Pentium Architecture,Superscalar Operation, Integer &Floating-Point Pipeline Stages, Branch Prediction Logic,Cache Organization

Comparative study of 8085, 80385, Pentium I, Pentium II and Pentium III,Pentium 4: Net burst micro architecture.Instruction translation look aside buffer and branch prediction

**References:**

1 John Uffenbeck, “8086/8088 family: Design Programming and Interfacing”, PHI.

2 Yu-Cheng Liu, Glenn A. Gibson, “Microcomputer System: The 8086/8088 Family,

Architecture, Programming and Design”, Prentice Hall

3 Walter A. Triebel, “The 80386DX Microprocessor: hardware, Software and Interfacing”,

Prentice Hall

4 Tom Shanley and Don Anderson, “Pentium Processor System Architecture”, Addison-

Wesley.

5 K. M. Bhurchandani and A. K. Ray, “Advanced Microprocessors and Peripherals”,

McGraw Hill

**Additional References:**

1 Barry B. Brey, “Intel Microprocessors”, 8thEdition, Pearson Education India

2 Douglas Hall, “Microprocessor and Interfacing”, Tata McGraw Hill.

3 Intel Manual

4 Peter Abel, “IBM PC Assembly language and Programming”, 5th Edition, PHI

5 James Antonakons, “The Pentium Microprocessor”, Pearson Education